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10/566,221	09/20/2006	Hajime Nagai	1176/309	5690

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EXAMINER	
TRAN, THIENVU V	
ART UNIT	PAPER NUMBER
2819	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,221	NAGAI, HAJIME	
	Examiner	Art Unit	
	Thienvu V. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 9-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,9-11 and 20-22* is/are rejected.

7)☐ Claim(s) *12-19,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/26/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. **Claims 1-2, 9-11, 20-22** are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's admitted prior art (hereinafter "AAPA").

Regarding claim 1, AAPA teaches a converting device (fig. 1) comprising:

a first input portion (In1) (fig. 1) receiving a first input signal (Si1) (fig. 1);

a first output portion (Out1) (fig. 1) outputting a first output signal (So1) (fig. 1); and a second input portion (In2) (fig. 1) receiving a second input signal (Si2) (fig. 1);

a second output portion (Out2) (fig. 1) outputting a second output signal (So2) (fig. 1); and

a voltage dropping circuit (e.g., 2, 3) (fig. 1) dropping voltages on a first node (N1) (fig. 1) located between said first input portion and said first output portion (see fig. 1) and a second node (N2) (fig. 1) located between said second input portion and said second output portion (see fig. 1) before changing from a state in which said first input portion is disconnected from said first node to a state in which said first input portion is connected to said first node (i.e., when transistors

2, 3 are turned on, a small voltage drop will appear at node N1 and N2 before they turn off again, thus, disconnecting the first input portion with the first node or the second input portion with the second node) (see fig. 1).

Regarding claim 2, AAPA teaches a voltage converting device (fig. 1) for receiving a first input signal (Si1) (fig. 1) having a first high input voltage and a first low input voltage (i.e., first input signal could either be a high or low signal) (fig. 1) and a second input signal (Si2) (fig. 1) having a second high input voltage and a second low input voltage (i.e., second input signal could either be a high signal or low signal) (fig. 1), said first high input voltage having a relatively high voltage level and said first low input voltage having a relatively low voltage level (see fig. 2), and said second high input voltage having a relatively high voltage level and said second low input voltage having a relatively low voltage level (see fig. 2), wherein said voltage converting device converts at least one of said first high input voltage and said first low input voltage and outputs said first input signal having a converted voltage level as a first output signal (So1) (fig. 1, 2) and converts at least one of said second high input voltage and said second low input voltage and outputs said second input signal having a converted voltage level as a second output signal (So2) (fig. 1, 2), wherein said voltage converting device comprises:

a first input portion (In1) (fig. 1) for receiving said first input signal (Si1) (fig. 1);

a first output portion (Out1) (fig. 1) for outputting said first output signal (i.e., So1) (fig. 1); and

a second input portion (In2) (fig. 1) receiving said second input signal (Si2) (fig. 1);

a second output portion (Out2) (fig. 1) outputting said second output signal (i.e., So2) (fig. 1); and

a voltage converting circuit converting at least one of said first high input voltage and said first low input voltage and at least one of said second high input voltage and said second low input voltage, and wherein said voltage converting circuit comprises a first voltage dropping circuit (2) (fig. 1) dropping a voltage on a first node (N1) (fig. 1) located between said first input portion and said first output portion (see fig. 1) before changing from a state in which said first input portion is disconnected from said first node to a state in which said first input portion is connected to said first node (i.e., when transistor 2 is turned on, a small voltage drop will appear at node N1 before it turns off again, thus, disconnecting the first input portion with the first node) (see fig. 1); and,

a second voltage dropping circuit (3) (fig. 1) dropping a voltage on a second node (N2) (fig. 1) located between said second input portion and said second output portion (see fig. 1) before changing from a state in which said second input portion is disconnected from said second node to a state in which said second input portion is connected to said second node (i.e., when transistor 3 is turned

on, a small voltage drop will appear at node N2 before it turns off again, thus, disconnecting the second input portion with the second node) (see fig. 1).

Regarding claim 9, AAPA teaches the voltage converting circuit comprises first conversion voltage supplying part (21) (fig. 1) supplying the first node with a first conversion voltage to convert one of the first high input voltage and the first low input voltage (i.e., power supply 21 supplies high voltage to node N1) (see fig. 1), the first conversion voltage having a higher voltage level than the first high input voltage (see background, DESCRIPTION OF RELATED ART, lines 26-28), and wherein the first voltage dropping circuit drops a voltage on the first node (i.e., when transistor 2 is asserted, a voltage drop will be at node N1) (see fig. 1), before changing from a state in which the first input portion is disconnected from the first node and the first conversion voltage supplying part is connected to the first node (i.e., when transistor 2 is deasserted, the first input portion will be disconnected from the first node N1 and the power supply 21 will be connected to the first node N1 through inverter 12) (see fig. 1) to a state in which the first input portion is connected to the first node (i.e., when transistor 2 is asserted, the first input portion will be connected to node N1) (see fig. 1).

Regarding claim 10, AAPA teaches the voltage converting circuit comprises second conversion voltage supplying part (22) (fig. 1) for supplying the first node with a second conversion voltage to convert the other of the first high input voltage and the first low input voltage (i.e., the second supplying voltage, ground, is connected to first node N1 through inverter 11) (see fig. 1), the second

conversion voltage having a voltage level lower than or equal to the first high input voltage (see background, DESCRIPTION OF RELATED ART, lines 28-29), and wherein the first voltage dropping circuit connects the second conversion voltage supplying part instead of the first conversion voltage supplying part to the first node (i.e., when transistor 2 is deasserted, the first node N1 is connected to power supply 22, ground, through pull-down transistor in inverter 11) (see fig. 1), before changing from a state in which the first input portion is disconnected from the first node and the first conversion voltage supplying part is connected to the first node (i.e., when transistor 2 is deasserted, the first input portion will be disconnected from the first node and power supply 21 will be connected to the first node N1 through inverter 12) (see fig. 1) to a state in which the first input portion is connected to the first node (i.e., when transistor 2 is asserted, the first input portion will be connected to first node N1) (see fig. 1).

Regarding claim 11, AAPA teaches the voltage converting circuit comprises third conversion voltage supplying part (21) (fig. 1) for supplying the second node with a third conversion voltage to convert one of the second high input voltage and the second low input voltage (i.e., the second node N2 is connected to power supply 21 through inverter 12) (see fig. 1) the third conversion voltage having a higher voltage level than the second high input voltage (see background, DESCRIPTION OF RELATED ART, lines 26-28), and wherein the second voltage dropping circuit drops a voltage on the second node (i.e., when transistor 3 is asserted, a voltage drop is at node N2) (see fig. 1), before

changing from a state in which the second input portion is disconnected from the second node and the third conversion voltage supplying part is connected to the second node (i.e., when transistor 3 is deasserted, the second input portion will be disconnected from second node N2) (see fig. 1) to a state in which the second input portion is connected to the second node (i.e., when transistor 3 is asserted, the second input portion will be connected to node N2) (see fig. 1).

Regarding claim 20, AAPA teaches the first input signal having a first high input voltage and a first low input voltage (i.e., the input voltage is either a high signal or low signal) (fig. 1), said first high input voltage having a relatively high voltage level and said first low input voltage having a relatively low voltage level (see fig 1, fig. 2), and said second input signal having a second high input voltage and a second low input voltage (i.e., second input is either a high signal or low signal) (fig. 1), said second high input voltage having a relatively high voltage level and said second low input voltage having a relatively low voltage level (see fig. 1, fig. 2).

Regarding claims 21, 22, they are rejected for the same reasons as stated in claims 9, 10, above.

Response to Arguments

3. Applicant's arguments filed 7/10/2007 have been fully considered but they are not persuasive.

The Examiner respectfully disagrees with the Applicant's statement citing "*AAPA does not teach or disclose the voltages on the nodes N1 and N2 are both dropped by*

voltage dropping circuit (e.g., TFT 5 and 6 in the disclosed embodiments)." Applicant is respectfully reminded that claims are interpreted in light of specification. Although the above elements are found as examples or embodiments in the specification, they were not claimed explicitly. Nor were the words that are used in the claims defined in the specification to require these limitations. A reading of the specification provides no evidence to indicate that the limitations must be imported into the claims to give meaning to disputed terms. *Constant v. Advanced MicroDevices Inc., 7USPQ 2d 1064.*

The Examiner respectfully submits that AAPA anticipates all claimed recitations of **claims 1-2, 9-11, 20-22** as set forth in the above detailed action. The rejection of **claims 1-2, 9-11, 20-22** is maintained.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Allowable Subject Matter

5. **Claims 12-19, 23-24** objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thienvu V. Tran whose telephone number is (571) 270-1276. The examiner can normally be reached on Monday-Friday (7:30AM-5:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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REXFORD BARNIE
SUPERVISORY PATENT EXAMINER
10/01/07